SLG4AC42401

Dual OSFP Low-Speed Host Controller

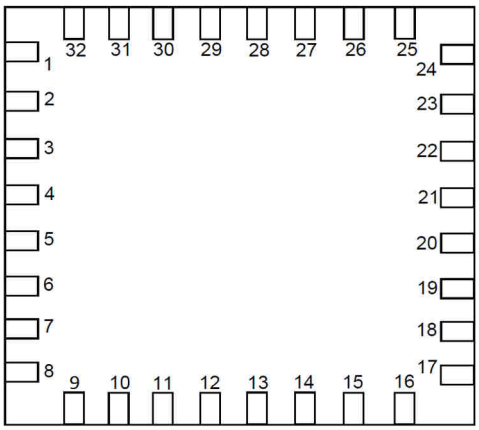
General Description

Dialog SLG4AC42401 is a low power and small form-factor bidirectional interface device for host-side low-speed OSFP standard interfaces based on a Dialog GreenPAK configurable mixed-signal IC. The device is available in a 4mm x 4mm STQFN package.

Features

- Dual channel OSFP module specification V1.2 compliant low-speed host side interface support
- Integrated INT/RSTn and HPW/PRSn detection and generation
- Low Power Consumption
- Pb - Free / RoHS Compliant, Halogen - Free
- STQFN – 32-Pin Package

Pin Configuration



STQFN-32 (Top view)

Table 1: Dialog OSFP Compatible Parts

Part Number	Description
SLG4AC42401	Dual OSFP Low-Speed Host Controller
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Table 2: Pin Name

Pin #	Pin Name	Pin #	Pin Name
1	RST_L_1	17	NC
2	HPW_1	18	H_INTn_1
3	H_PRSn_0	19	NC
4	H_INTn_0	20	H_PRSn_1
5	H_RSTn_0	21	H_RSTn_1
6	H_LPW_0	22	H_LPW_1
7	NC	23	NC
8	H_INTn_invert	24	NC
9	H_RSTn_invert	25	HPW_0
10	H_PRSn_invert	26	INT_RSTn_0
11	HPW_invert	27	HPW_PRS_0
12	NC	28	INT_RSTn_1
13	NC	29	HPW_PRS_1
14	GND	30	GND
15	VDD2	31	VDD
16	NC	32	RST_L_0

Table 3: Ordering Information

Part Number	Package Type
SLG4AC42401V	32-pin STQFN
SLG4AC42401VTR	32-pin STQFN - Tape and Reel (3k units)

Block Diagram

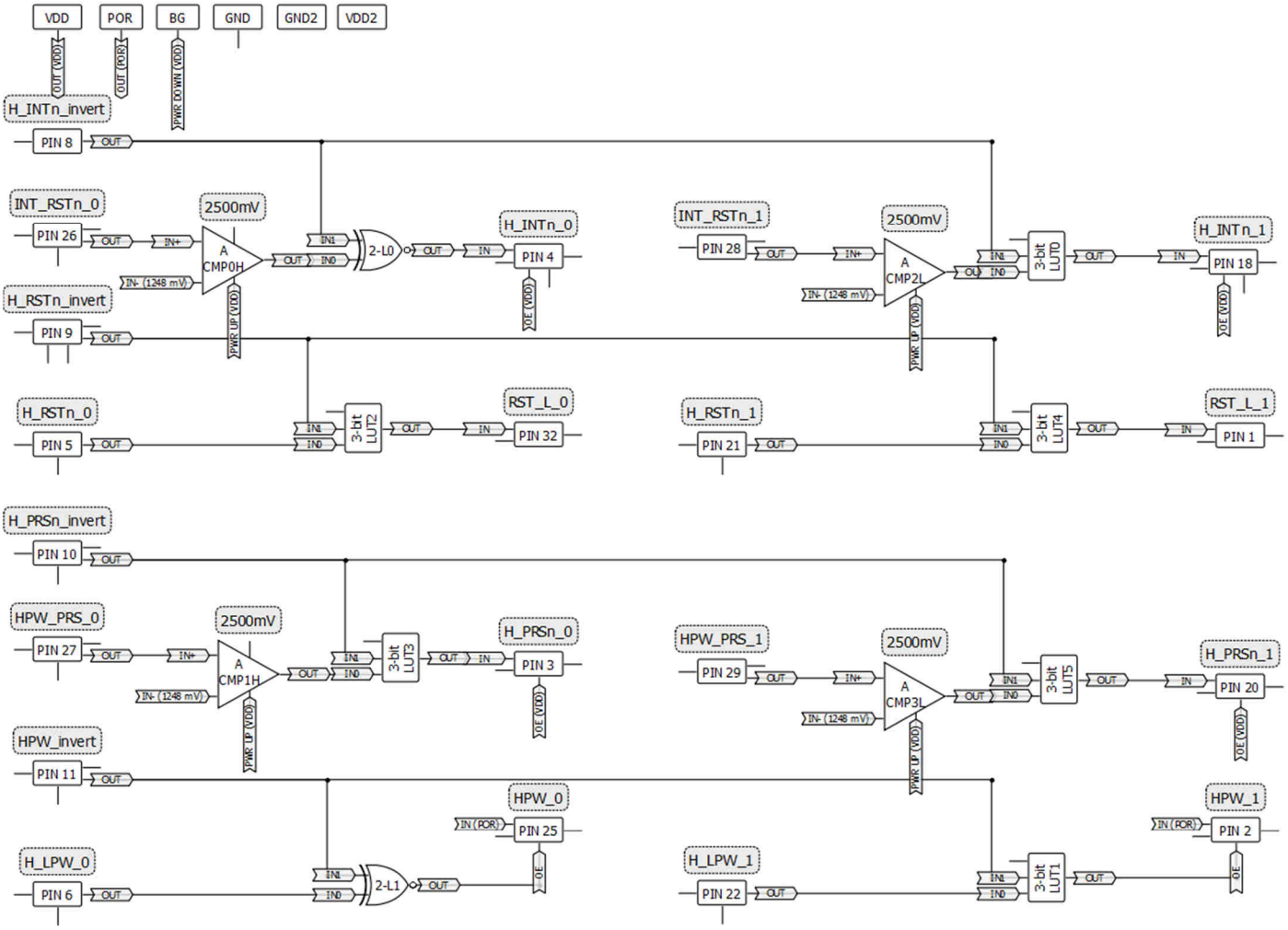


Figure 1: SLG4AC42401 internal block diagram

Table 4: Pin Configuration

Pin #	Pin Name	Type	Pin Description	Default Polarity
1	RST_L_1	Digital Output	Output to drive INT_RSTn_1 line to reset the Module	Active Low
2	HPW_1	Digital Output	Output to drive HPW_PRSn_1 line to High Power Mode	Active High
3	H_PRSn_0	Digital Output	Signal to Host that Module is Present	Active Low
4	H_INTn_0	Digital Output	Signal to Host that Module sent Interrupt	Active Low
5	H_RSTn_0	Digital Input	Host control to GPAK to assert Module Reset	Active Low
6	H_LPW_0	Digital Input	Host control to GPAK to assert Module Low Power Mode	Active High
8	H_INTn_invert	Digital Input	Input to invert both H_INTn default polarities	N/A
9	H_RSTn_invert	Digital Input	Input to invert both H_RSTn default polarities	N/A
10	H_PRSn_invert	Digital Input	Input to invert both H_PRSn default polarities	N/A
11	HPW_invert	Digital Input	Input to invert both HPW default polarities	N/A
14	GND	GND	Ground	
15	VDD2	PWR	Supply Voltage. Connect to the same rail as VDD.	
18	H_INTn_1	Digital Output	Signal to Host that Module sent Interrupt	Active Low
20	H_PRSn_1	Digital Output	Signal to Host that Module is Present	Active Low
21	H_RSTn_1	Digital Input	Host control to GPAK to assert Module Reset	Active Low
22	H_LPW_1	Digital Input	Host control to GPAK to assert Module Low Power Mode	Active High
25	HPW_0	Digital Output	Output to drive HPW_PRSn_0 line to High Power Mode	Active High
26	INT_RSTn_0	Analog Input/Output	OSFP slow speed signal	
27	HPW_PRS_0	Analog Input/Output	OSFP slow speed signal	
28	INT_RSTn_1	Analog Input/Output	OSFP slow speed signal	
29	HPW_PRS_1	Analog Input/Output	OSFP slow speed signal	
30	GND	GND	Ground	
31	VDD	PWR	Supply Voltage. Connect to the same rail as VDD2.	
32	RST_L_0	Digital Output	Output to drive INT_RSTn_0 line to reset the Module	Active Low
7, 12, 13, 16, 17, 19, 23, 24	NC	--	Connect to GND	

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage to GND	-0.3	7	V
V_I	Voltage at Input Pin	-0.3	7	V
I_{MAX}	Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
I_{lkg}	Input leakage Current (Absolute Value)	--	1.0	µA
T_{STRG}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature	--	150	°C
T_{AMB}	Ambient operating temperature	-40	+85	°C
ESD	ESD Protection (Human Body Model)	±2000	--	V
	ESD Protection (Charged Device Model)	±1300	--	V
MSL	Moisture Sensitivity Level	1		

Table 6: Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
V_{DD2}	Supply Voltage		3	3.3	3.6	V
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	69	--	µA
V_{IH}	HIGH-Level Input Voltage	Logic Input at V_{DD}=3.3V	0.7*V_{DD}	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input at V_{DD}=3.3V	GND-0.3	--	0.3*V_{DD}	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, IOH=3mA at V_{DD}=3.3V	2.7	2.79	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at V_{DD}=3.3V	--	0.158	0.217	V
		Open Drain NMOS 1X, I_{OL}=3mA, at V_{DD}=3.3V	--	0.063	0.087	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, VOH=2.4V at V_{DD}=3.3V	5.54	7.48	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.4V, at V_{DD}=3.3V	5.26	7.00	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at V_{DD}=3.3V	12.90	17.14	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 6, 22	7	--	17	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 5, 21	7	--	17	kΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{ACMP}	Analog Comparator 0, 1, 2, 3 Threshold Voltage	Low to High transition, at temperature -40 +85°C (Note 3)	--	2496	--	mV
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.13	1.72	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. Guaranteed by Design.
3. Pins 1-9, 20-29, and 32 are powered from V_{DD}, and Pins 10-13, 16-19 are powered from V_{DD2}

Description

The SLG4AC42401 Dual OSFP Low-Speed Host Controller device contains two pairs of INT_RSTn and HPW_PRS signals transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when M_RSTn is asserted low. The module (SLG4AX42397) signals an interrupt to the host when M_INT_L is asserted low.

HPW_PRS is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG4AX42397) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when M_RSTn is asserted low.

For ease of system use, four invert input pins have been added to invert the default polarity of output signals. Refer to Table 7.

Table 7: Output Polarity Control

Invert Pin Name	Status	Output Polarity
H_INTn_invert	Low	Active Low
	High	Active High
H_RSTn_invert	Low	Active Low
	High	Active High
H_PRSn_invert	Low	Active Low
	High	Active High
HPW_invert	Low	Active High
	High	Active Low

Table 8: Dialog Compatible OSFP Parts

Part Number	Description
SLG4AC42401	Dual OSFP Low-Speed Host Controller
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Typical Application Circuit

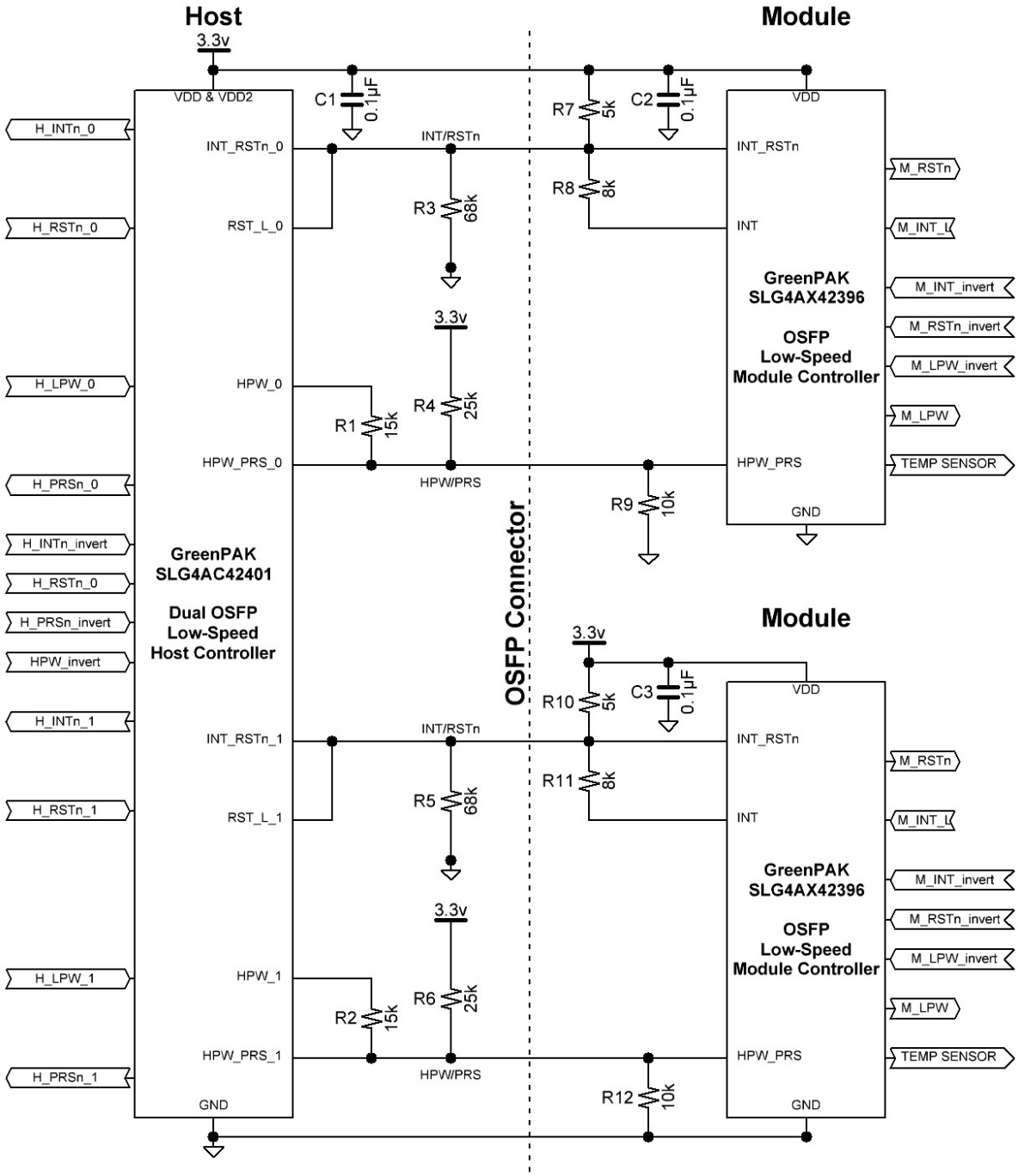


Figure 2: SLG4AC42401 Typical Application Circuit

Package Top Marking

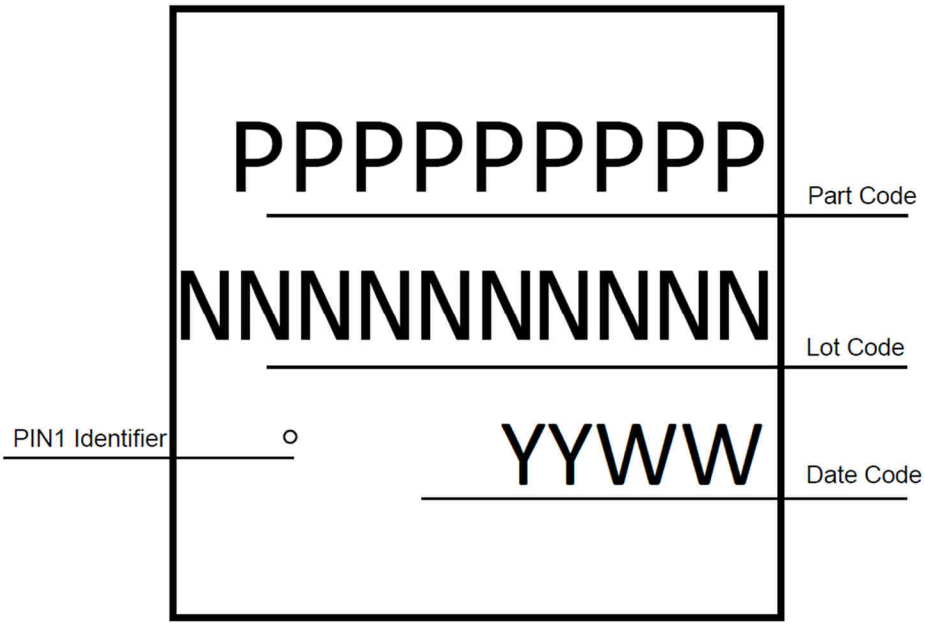


Figure 3: Package Top Marking

Table 9: Part Information

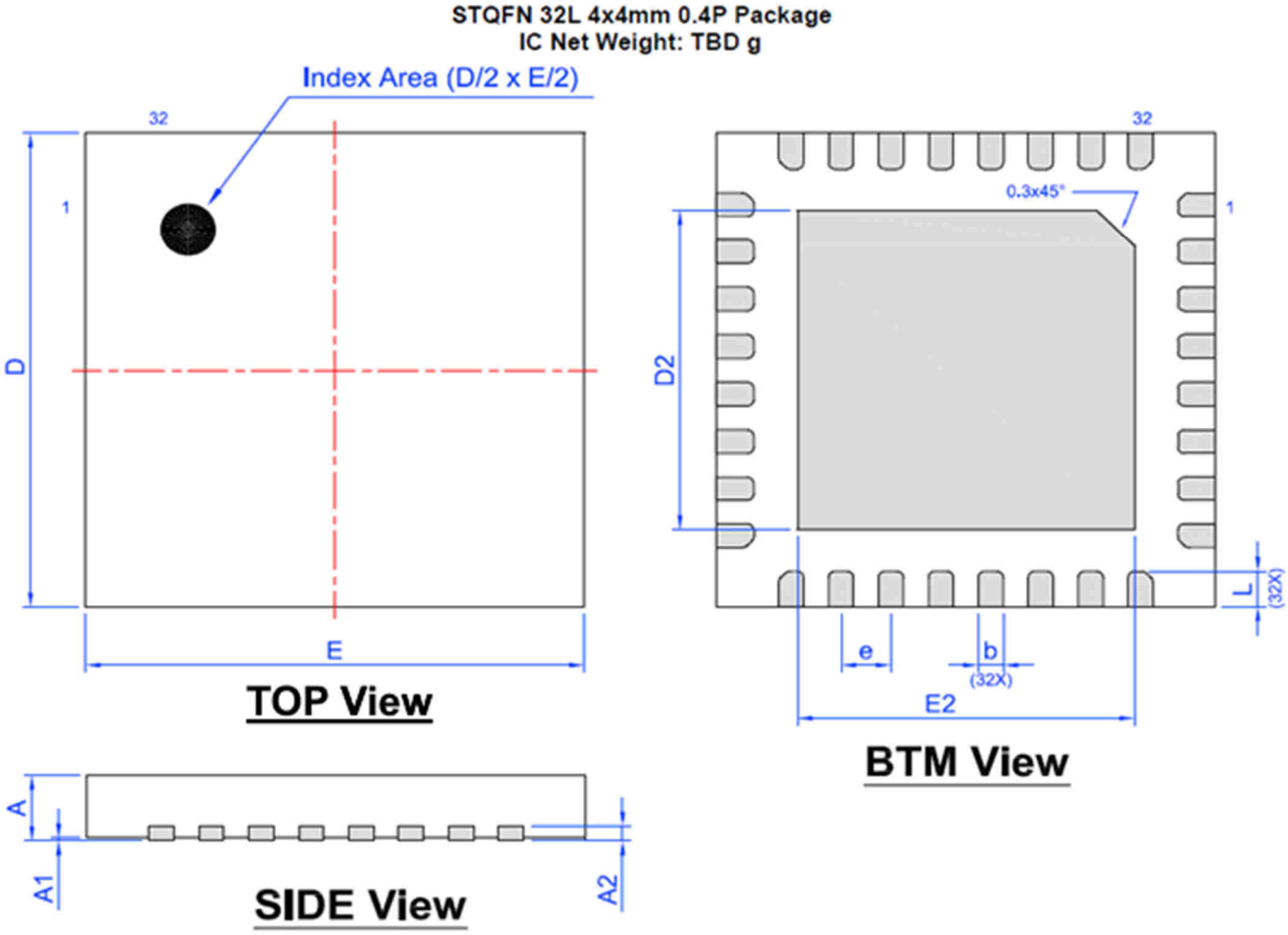
Datasheet Revision	Programming Code Number	Locked Status	Checksum	Part Code	Revision	Date
0.15	005	U	0x79DA96E9			07/25/2018

Table 10: Lock Status

Lock Status	
X	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

The IC security bit is locked/set for code security for production unless otherwise specified.
The Revision number is not changed for bit locking.

Package Drawing and Dimensions



Unit: mm

Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	3.950	4.000	4.050
A1	0.00	-	0.050	E	3.950	4.000	4.050
A2	0.150 REF			D2	2.650	2.700	2.750
b	0.150	0.200	0.250	E2	2.650	0.270	2.750
e	0.400 BSC			L	0.250	0.300	0.350

Figure 4: SLG4AC42401 Package Drawing and Dimensions

Table 11: Tape and Reel Specification

Package Type	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
		per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 32L 4x4 mm 0.4P Green	4 x 4 x 0.55	5000	10000	330/100	42	336	42	336	12	8

Table 12: Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 4x4 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12

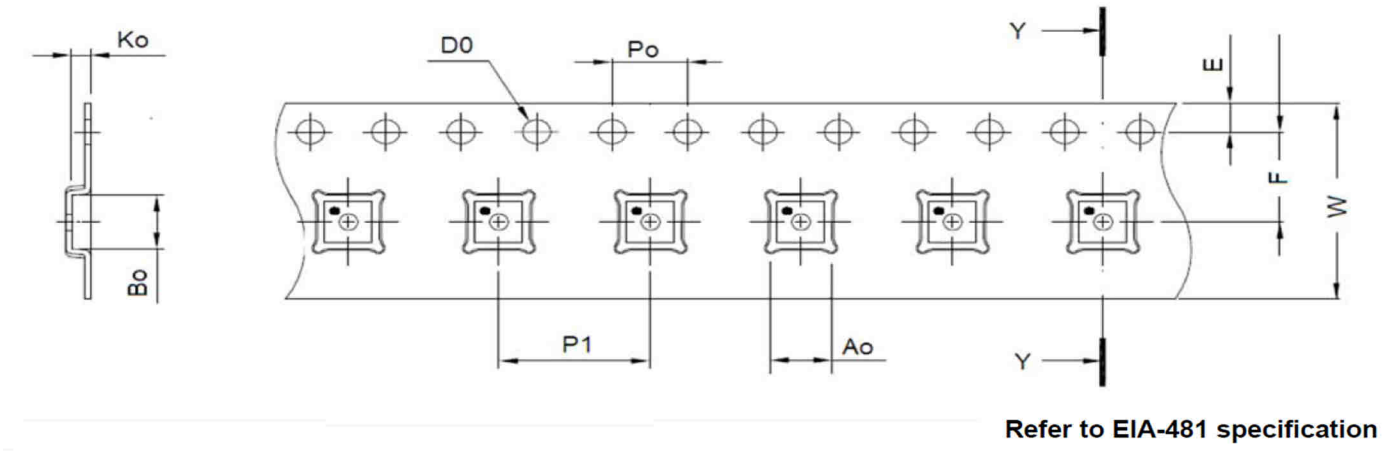


Figure 5: Tape Dimensions

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

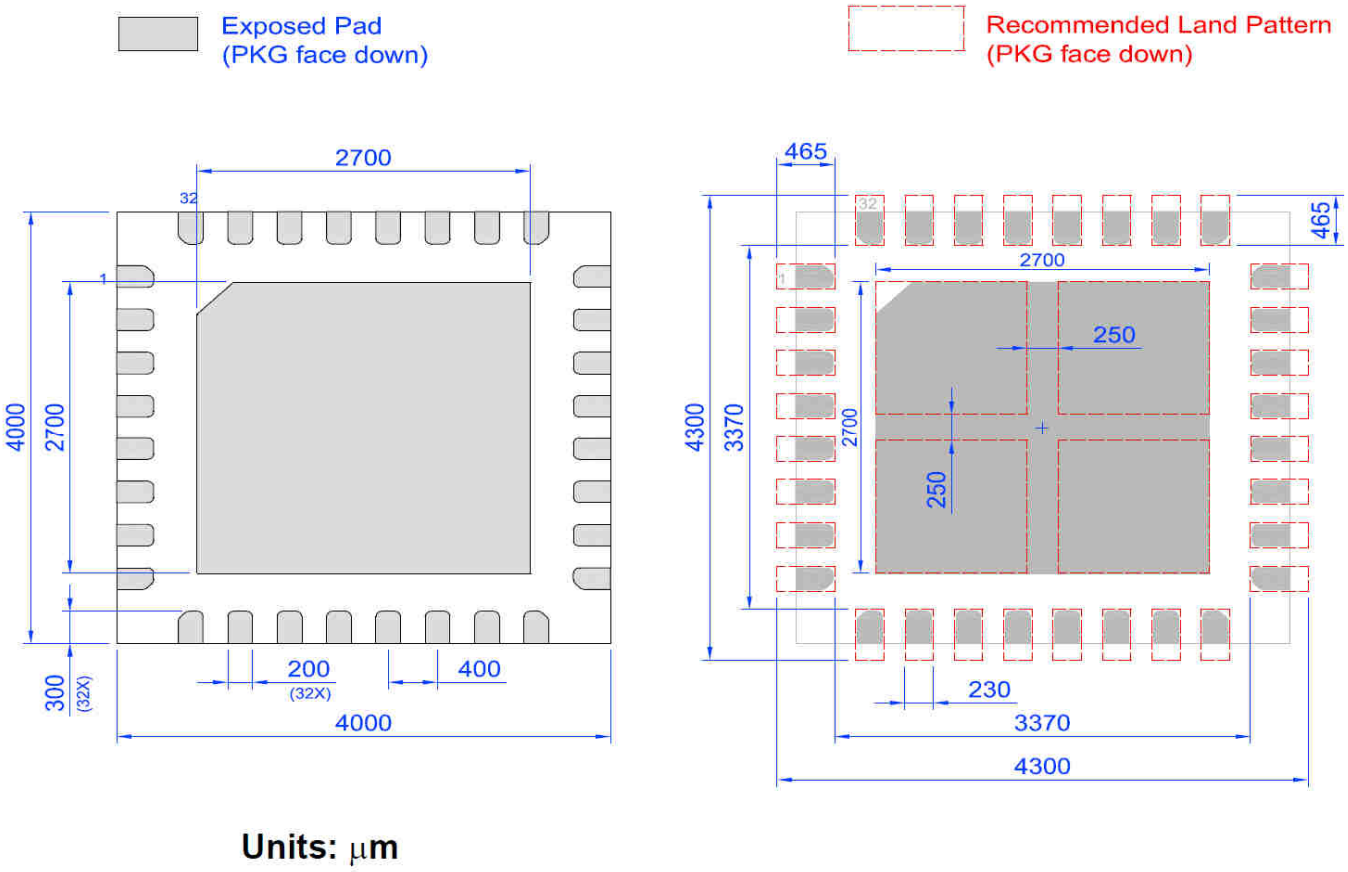


Figure 6: SLG4AC42401 Recommended Land Pattern

Table 13: Datasheet Revision History

Date	Version	Change
04/02/2018	0.10	New design for SLG46880 chip based on SLG4P42332
04/23/2018	0.11	Updated DS formatting
04/23/2018	0.12	Updated HPW polarity
05/02/2018	0.13	Updated DS formatting
05/04/2018	0.14	Updated DS formatting
07/25/2018	0.15	Updated pinout and added inverting functionality

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