SLG4AX42396

GreenPAK ™

OSFP Low-Speed Host Controller

General Description

Renesas SLG4AX42396 is a low power and small form-factor bidirectional interface device for host-side low-speed OSFP standard interfaces based on a Renesas GreenPAK configurable mixed-signal IC. The device is available in a 1.6mm x 2.0mm STQFN package.

Features

- OSFP module specification V2.0 compliant low-speed host side interface support
- Integrated INT/RSTn and LPWn/PRSn detection and generation
- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Pin Configuration

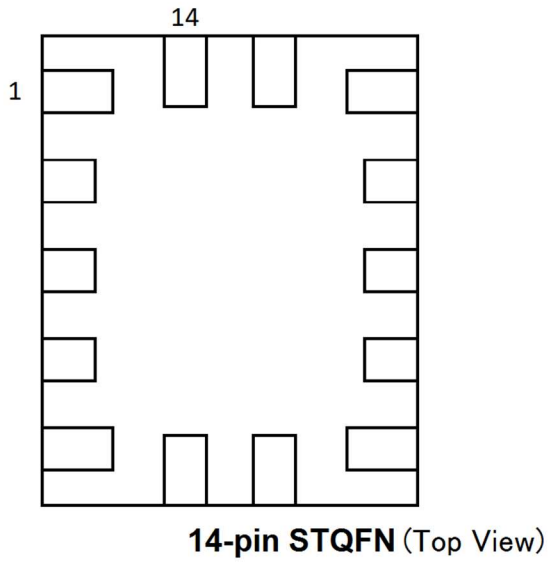


Figure 1: Pin Layout

Table 1: Other Renesas OSFP Compatible Parts

Part Number	Description
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Table 2: Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	H_RSTn	9	LPWn_PRSn
3	H_INTn_invert	10	INT_RSTn
4	H_RSTn_invert	11	LPWn
5	H_PRSn_invert	12	H_LPWn
6	H_LPWn_invert	13	H_PRSn
7	RSTn	14	H_INTn

Table 3: Ordering Information

Part Number	Package Type
SLG4AX42396V	14-pin STQFN
SLG4AX42396VTR	14-pin STQFN - Tape and Reel (3k units)

Block Diagram

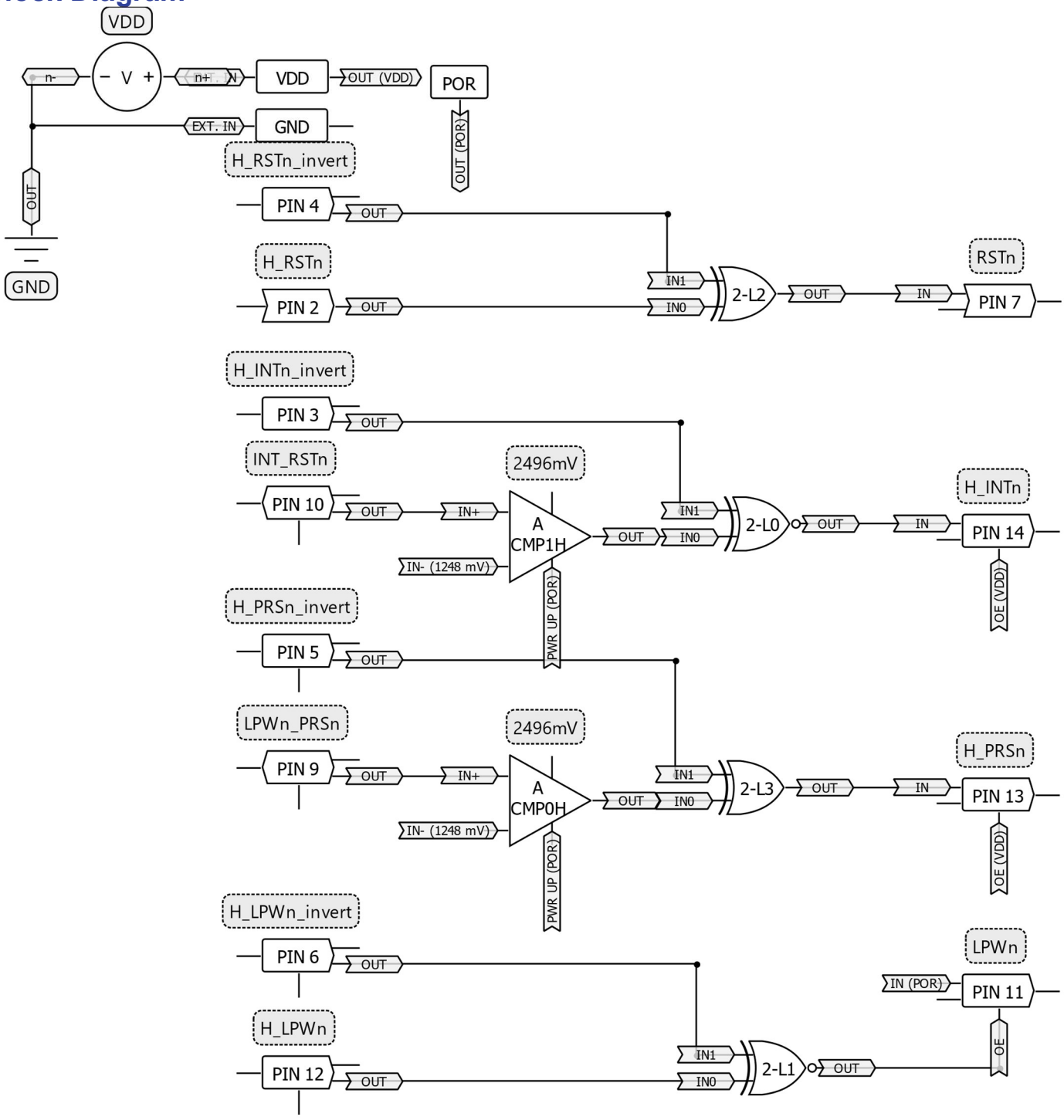


Figure 2. SLG4AX42396 internal block diagram

Table 4: Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	H_RSTn	Digital Input	Host control to GPAK to assert Module Reset	10kΩ pulldown
3	H_INTn_invert	Digital Input	Input to invert H_INTn (PIN14) polarity	floating
4	H_RSTn_invert	Digital Input	Input to invert H_RSTn (PIN2) polarity	floating
5	H_PRSn_invert	Digital Input	Input to invert H_PRSn (PIN13) default polarity	floating
6	H_LPWn_invert	Digital Input	Input to invert H_LPWn (PIN12) polarity	floating
7	RSTn	Digital Output	Output to drive INT_RSTn line to reset the Module	floating
8	GND	GND	Ground	--
9	LPWn_PRSn	Analog Input/Output	OSFP slow speed signal	floating
10	INT_RSTn	Analog Input/Output	OSFP slow speed signal	floating
11	LPWn	Digital Output	Output to drive LPWn_PRSn line for Low Power Mode	floating
12	H_LPWn	Digital Input	Host control to GPAK to assert Module Low Power Mode control	10kΩ pullup
13	H_PRSn	Digital Output	Signal to Host that Module is Present	floating
14	H_INTn	Digital Output	Signal to Host that Module sent Interrupt	floating

Table 5: Absolute Maximum Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage to GND	-0.3	7	V
V_I	Voltage at Input Pin	-0.3	7	V
I_{MAX}	Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
I_{lkg}	Input leakage Current (Absolute Value)	--	1.0	µA
T_{STRG}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature	--	150	°C
T_{AMB}	Ambient operating temperature	-40	+85	°C
ESD	ESD Protection (Human Body Model)	±2000	--	V
	ESD Protection (Charged Device Model)	±1300	--	V
MSL	Moisture Sensitivity Level	1		

Table 6: Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	57	--	µA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	0.7*V_{DD}	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	GND-0.3	--	0.3*V_{DD}	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.7	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at V_{DD}=3.3V	--	--	0.16	V
I_{OH}	HIGH-Level Output Current	Push-Pull 1X, V_{OH}=2.4V at V_{DD}=3.3V	5.29	--	--	mA
I_{OL}	LOW-Level Output Current	Push-Pull 1X, V_{OL}=0.4V, at V_{DD}=3.3V	4.68	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at V_{DD}=3.3V	12.07	--	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 12	6	--	14	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	6	--	14	kΩ
V_{ACMP}	Analog Comparator 0H Threshold Voltage	Low to High transition, at temperature -40 +85°C (Note 1)	2453	2496	2526	mV
		Low to High transition, at temperature 25°C (Note 1)	2462	2496	2526	mV

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
		High to Low transition, at temperature -40 +85°C (Note 1)	2453	2496	2526	mV
		High to Low transition, at temperature 25°C (Note 1)	2462	2496	2526	mV
	Analog Comparator 1H Threshold Voltage	Low to High transition, at temperature -40 +85°C (Note 1)	2450	2496	2525	mV
		Low to High transition, at temperature 25°C (Note 1)	2460	2496	2525	mV
		High to Low transition, at temperature -40 +85°C (Note 1)	2451	2496	2525	mV
		High to Low transition, at temperature 25°C (Note 1)	2461	2496	2524	mV
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note:
1. Guaranteed by Design.

Description

The SLG4AX42396 OSFP Low-Speed Host Controller device contains INT_RSTn and LPWn_PRSn signal transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when H_RSTn is asserted low. The module signals an interrupt to the host when H_INTn is asserted low.

LPW_PRS is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG4AX42397) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when H_LPWn is asserted low.

The MSA defines the multi-level signaling of the INT_RSTn and LPWn_PRSn lines. The MSA also defines the polarities of the Host and Module signals (i.e. M_RSTn, M_INT, H_INTn, H_LPWn). In order to guarantee the SLG4AX42396 operates with all polarities following the MSA spec, tie according to Table 7 below.

Table 7: Pullups/downs to conform to MSA Standard Polarities

Pin Name	Resistor
H_INTn_invert	1kΩ Pull Down
H_RSTn_invert	1kΩ Pull Down
H_PRSn_invert	1kΩ Pull Down
H_LPWn_invert	1kΩ Pull Up

Table 8: Other Dialog OSFP Compatible Parts

Part Number	Description
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Typical Application Circuit

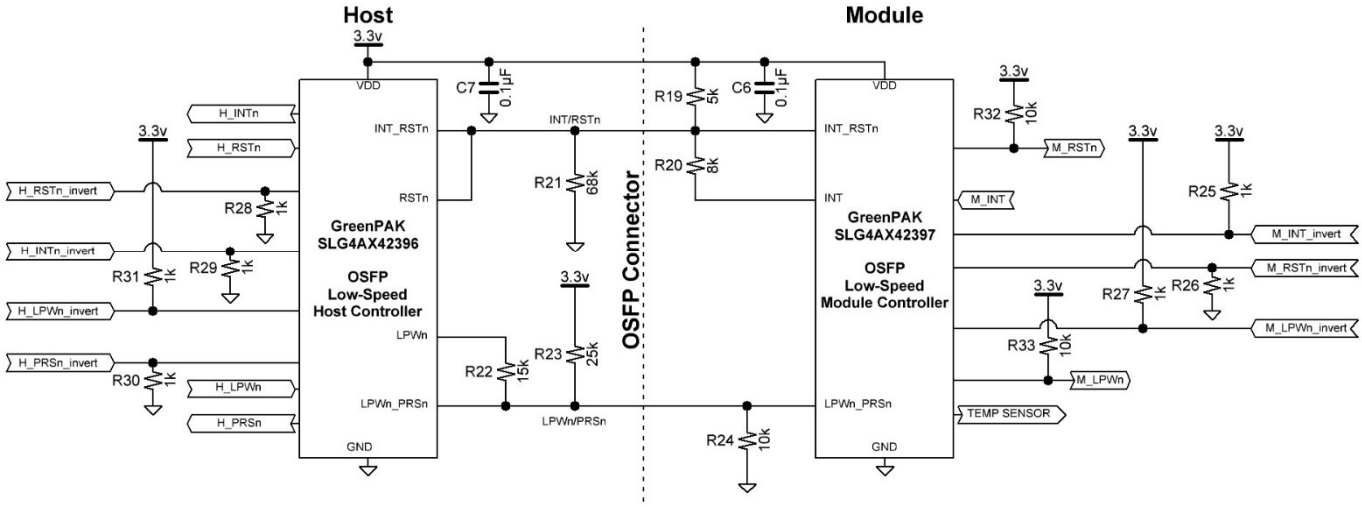


Figure 3: SLG4AX42396 Typical Application Circuit

Functionality Waveforms

Channel 1 (yellow/top line) – PIN#10 (INT_RSTn)
Channel 2 (light blue/2nd line) – PIN#2 (H_RSTn)
Channel 3 (magenta /3rd line) – PIN#14 (H_INTn)
Strapped according to Table 7 configuration.

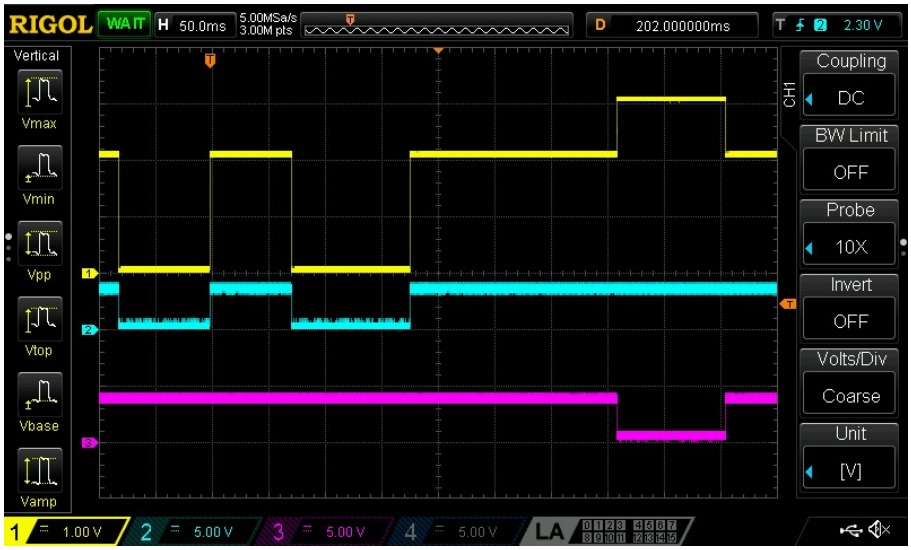


Figure 4 - INT_RSTn Functionality

Channel 1 (yellow/top line) – PIN#9 (LPWn_PRSn)
Channel 2 (light blue/2nd line) – PIN#12 (H_LPWn)
Channel 3 (magenta /3rd line) – PIN#13 (H_PRSn)
Strapped according to Table 7 configuration.

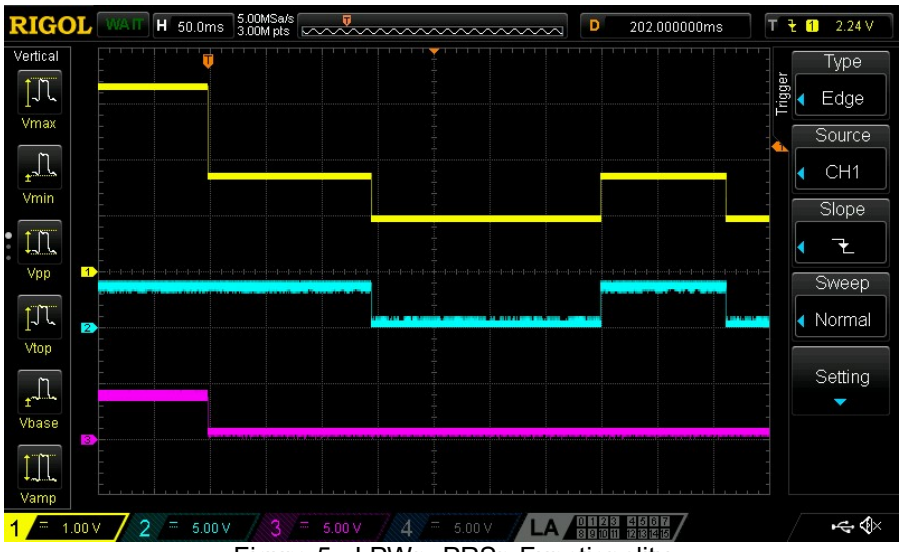


Figure 5 - LPWn_PRSn Functionality

Package Top Marking

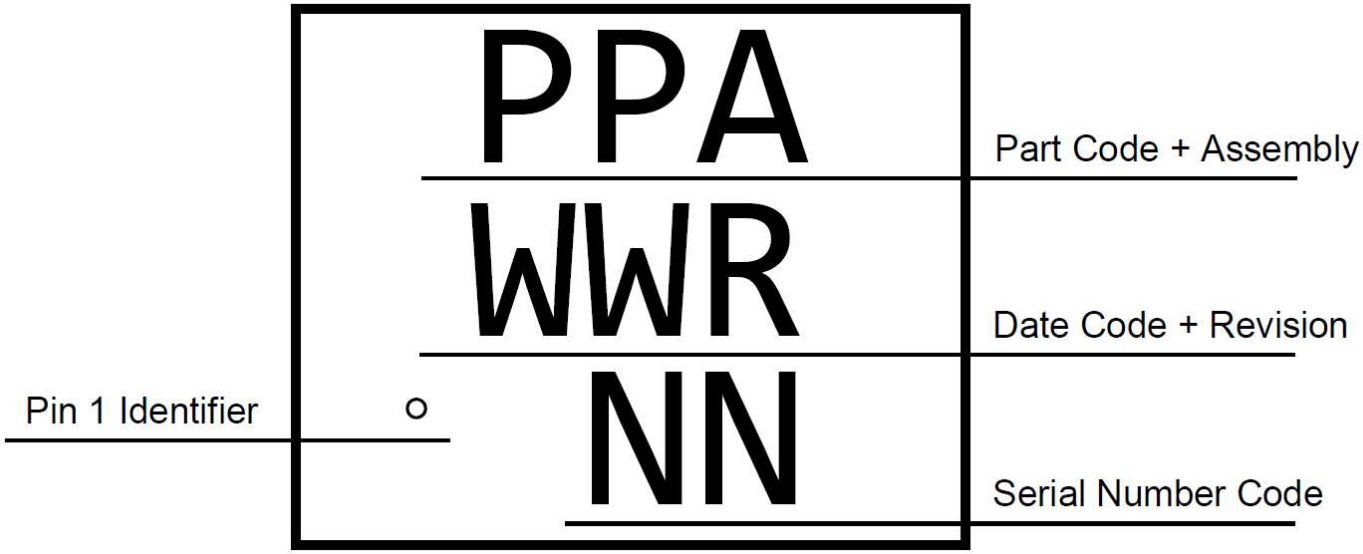


Figure 6. Package Top Marking

Table 9: Part Information

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	008	L	0x45001F19	1B	C	06/26/2023

Lock coverage for this part is indicated by √, from one of the following options:

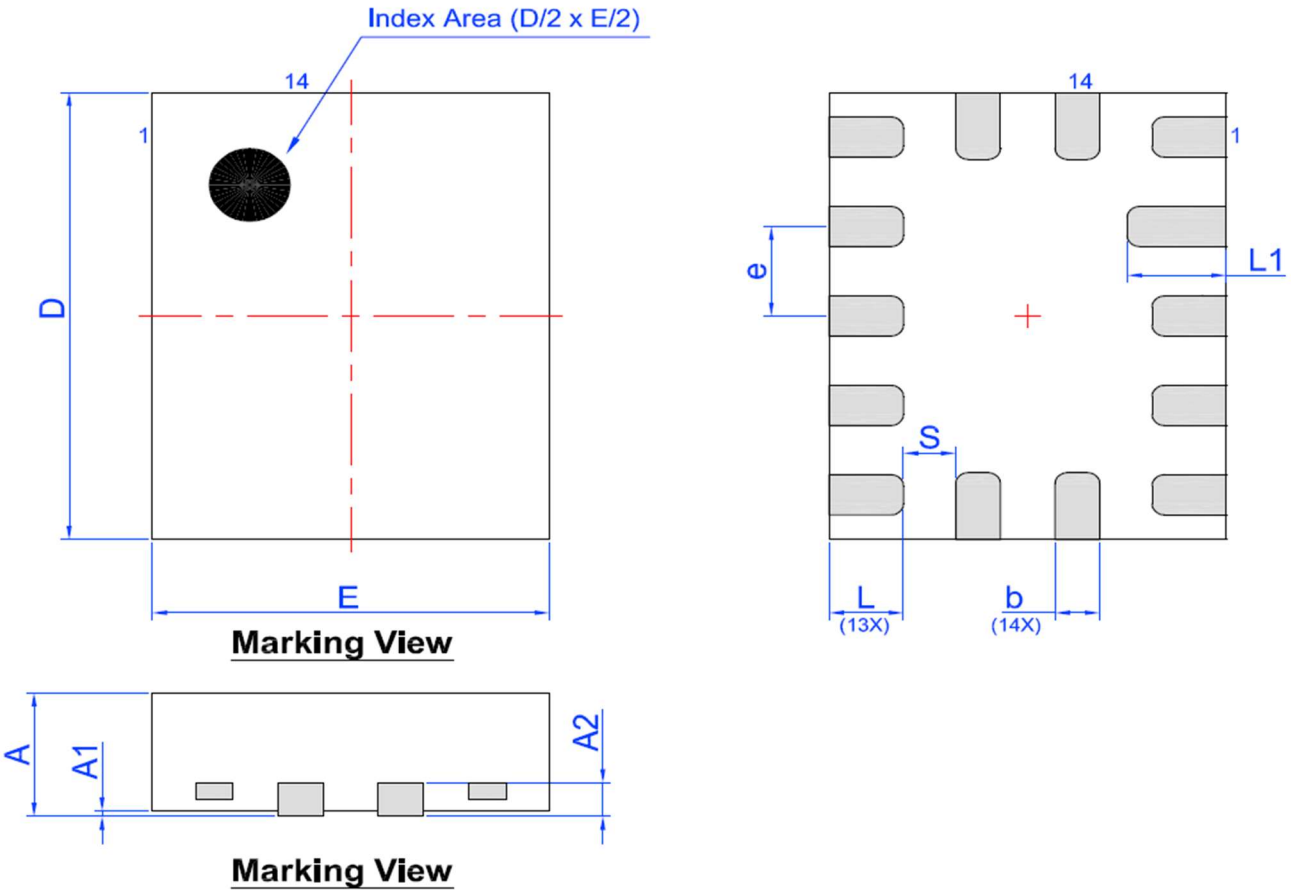
Table 10: Lock Status

	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
√	All lock read/write (mode 6)

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Figure 7. SLG4AX42396 Package Drawing and Dimensions

Table 11: Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Table 12: Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8

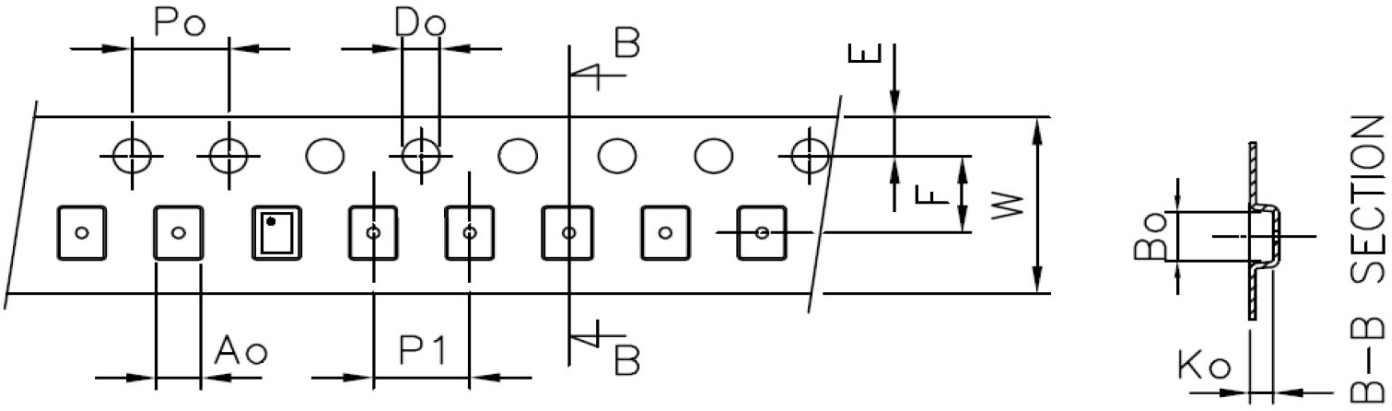


Figure 8. Tape Dimensions

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Layout Guidelines

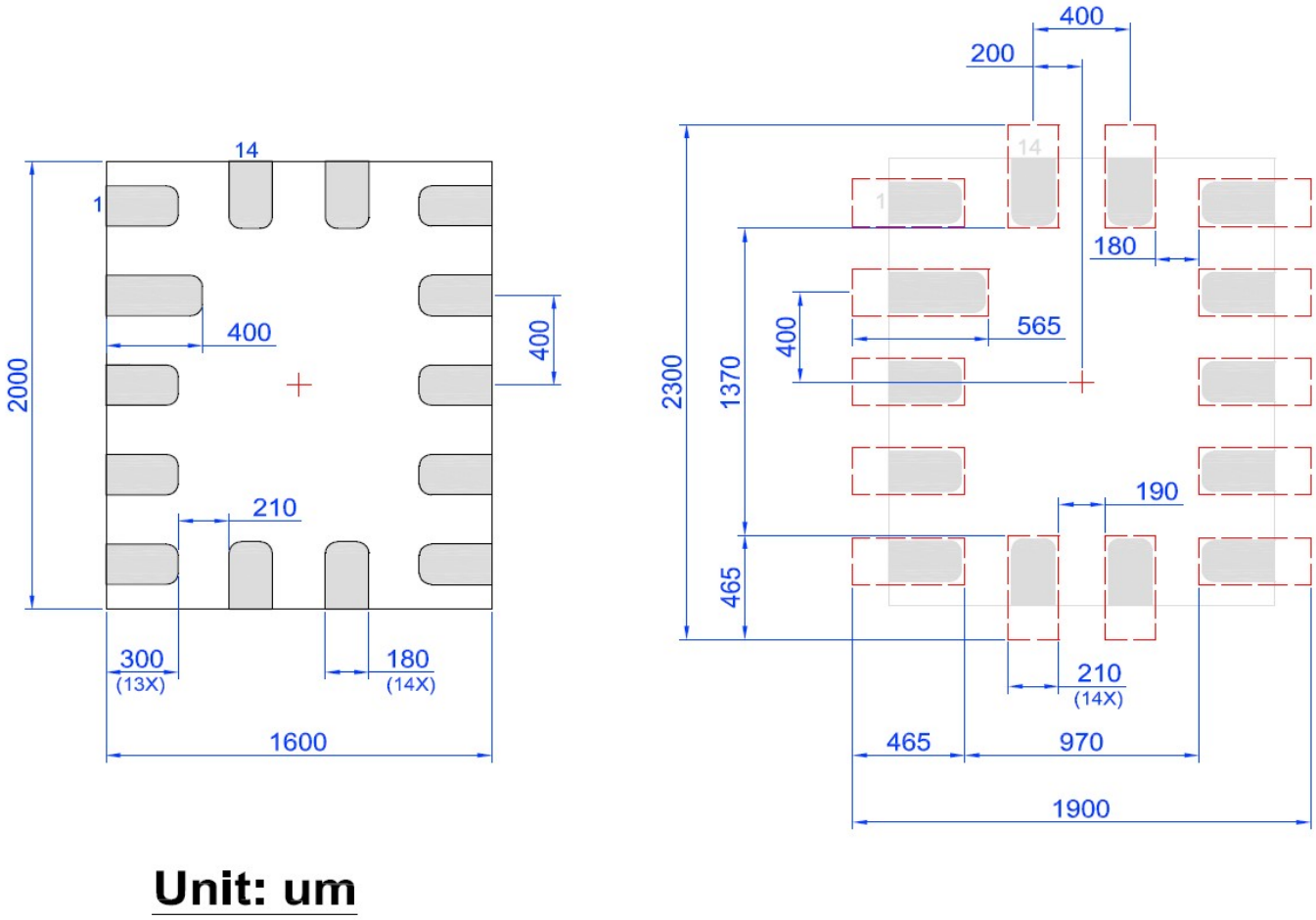


Figure 9. SLG4AX42396 Recommended Land Pattern

Table 13: Datasheet Revision History

Date	Version	Change
03/30/2018	0.10	New design for SLG46855 chip
07/25/2018	0.11	Updated DS formatting
08/28/2018	0.12	Updated DS formatting
11/16/2018	0.13	Updated Device Revision Table
12/13/2018	0.14	Updated typical application circuit and ACMP threshold voltage range
01/25/2019	0.15	Updated pin names and application circuit
01/29/2019	0.16	Changed PIN7 name from RST to RSTn and updated Typical Application Circuit
02/01/2019	0.17	Updated PIN6 name, typical application circuit, and functionality waveforms
02/05/2019	0.18	Updated Description
02/06/2019	0.19	Updated Pin Configuration and Description
02/13/2019	0.20	Updated Features to describe the correct OSFP module specification
06/27/2019	0.21	Updated Device Revision Table
04/27/2021	0.22	Updated Lock Status
05/12/2021	0.23	Updated Device Revision Table
05/13/2021	1.00	Production Release
06/26/2023	1.01	Moved to Renesas template