SLG4AX42397

GreenPAK ™

OSFP Low-Speed Module Controller

General Description

Renesas SLG4AX42397 is a low power and small form device. The SoC is housed in a 1.6mm x 2.0mm STQFN package which is optimal for using with small devices.

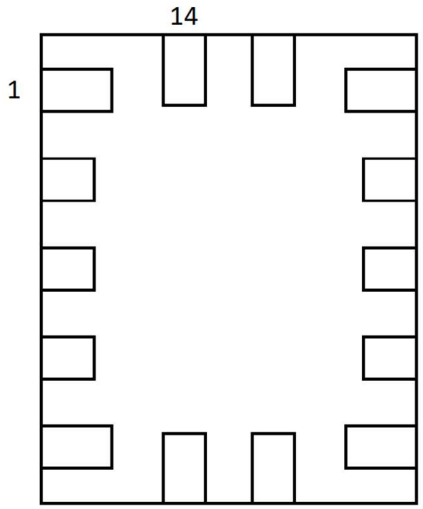
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Output Summary

3 Outputs - Open Drain NMOS 2X

Pin Configuration

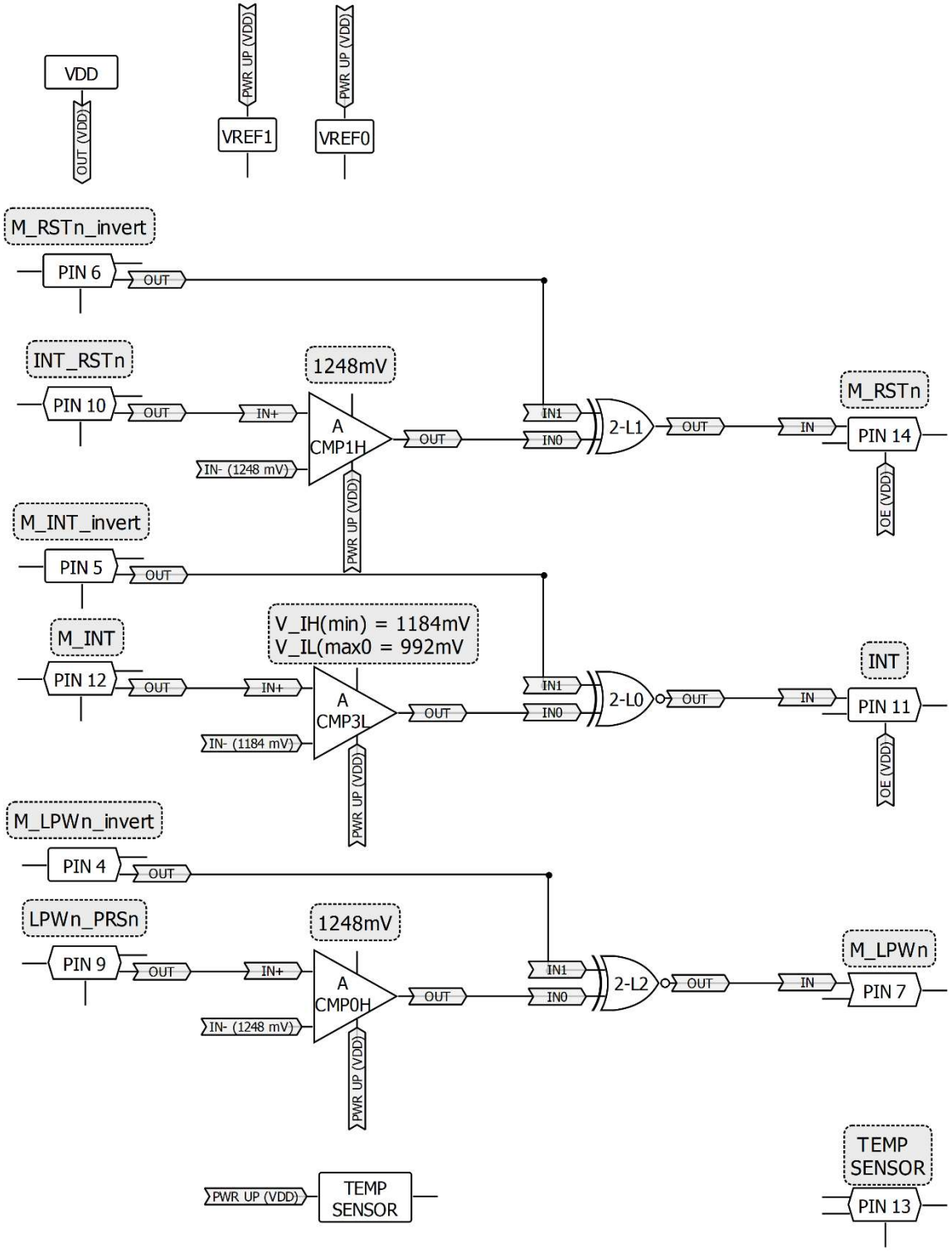


14-pin STQFN (Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	NC	9	LPWn_PRSn
3	NC	10	INT_RSTn
4	M_LPWn_invert	11	INT
5	M_INT_invert	12	M_INT
6	M_RSTn_invert	13	TEMP SENSOR
7	M_LPWn	14	M_RSTn

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	NC	--	Keep Floating or Connect to GND	--
4	M_LPWn_invert	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
5	M_INT_invert	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
6	M_RSTn_invert	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
7	M_LPWn	Digital Output	Open Drain NMOS 2X	floating
8	GND	GND	Ground	--
9	LPWn_PRSn	Analog Input/Output	Analog Input/Output	floating
10	INT_RSTn	Analog Input/Output	Analog Input/Output	floating
11	INT	Digital Output	Open Drain NMOS 2X	floating
12	M_INT	Analog Input/Output	Analog Input/Output	1MΩ pullup
13	TEMP SENSOR	Analog Input/Output	Analog Input/Output	floating
14	M_RSTn	Digital Output	Open Drain NMOS 2X	floating

Ordering Information

Part Number	Package Type
SLG4AX42397V	14-pin STQFN
SLG4AX42397VTR	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	V_{DD}+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	OD 2x	--	21	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PIN9 and PIN10 are LOW	--	71	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
V_{OL}	LOW-Level Output Voltage	Open Drain NMOS 2X, I_{OL}=3mA, at VDD=3.3V	--	--	0.046	V
I_{OL}	LOW-Level Output Current (Note 1)	Open Drain NMOS 2X, V_{OL}=0.4V, at VDD=3.3V	25.23	--	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 4, 5, 6	--	10	--	kΩ
		Pull up on PIN 12	--	1	--	MΩ
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	1237	1248	1260	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1234	1248	1263	mV
		High to Low transition, at temperature 25°C	1236	1248	1259	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1236	1248	1263	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	1232	1248	1263	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1232	1248	1265	mV
		High to Low transition, at temperature 25°C	1231	1248	1263	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1226	1248	1265	mV

V_{ACMP3}	Analog Comparator3 Threshold Voltage	Low to High transition, at temperature 25°C	1167	1184	1201	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1162	1184	1201	mV
		High to Low transition, at temperature 25°C	977	992	1007	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	971	992	1009	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 3)	ACMP 3 at temperature 25°C	188	192	197	mV
		ACMP 3 at temperature -40 +85°C	188	192	197	mV
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.

Description

The SLG4AX42397 OSFP Low-Speed Module Controller device contains INT_RSTn and LPWn_PRSn signal transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when M_RSTn is asserted low. The module signals an interrupt to the host when M_INT is asserted high.

LPWn_PRSn is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG4AX42397) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when M_LPWn is asserted low.

The equation below calculates the typical analog voltage passed from the temperature sensor to Pin 13 with chip to chip variation of about ±2°C:

$$V_{TS} = -2.8 \times T + 1077.2$$

The MSA defines the multi-level signaling of the INT_RSTn and LPWn_PRSn lines. The MSA also defines the polarities of the Host and Module signals (i.e. M_RSTn, M_INT, H_INTn, H_LPWn). In order to guarantee the SLG4AX42397 operates with all polarities following the MSA spec, tie according to Table 1 below.

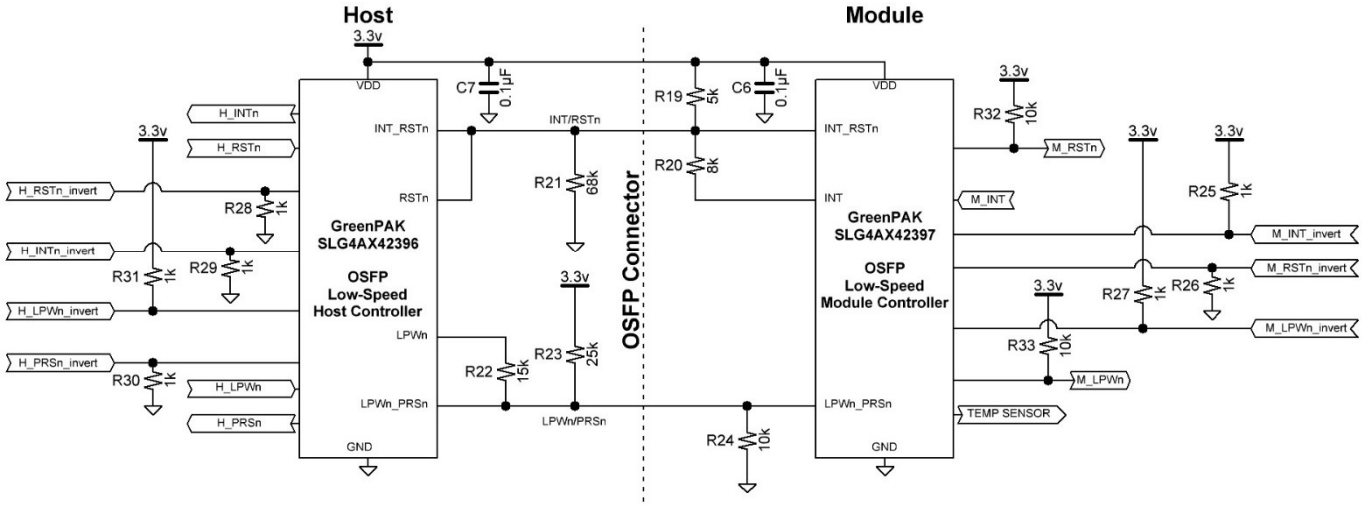
Table 1: MSA Polarities

Pin Name	Resistor
M_LPWn_invert	1kΩ Pull Up
M_INT_invert	1kΩ Pull Up
M_RSTn_invert	1kΩ Pull Down

Table 2: Other Dialog OSFP Compatible Parts

Part Number	Description
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

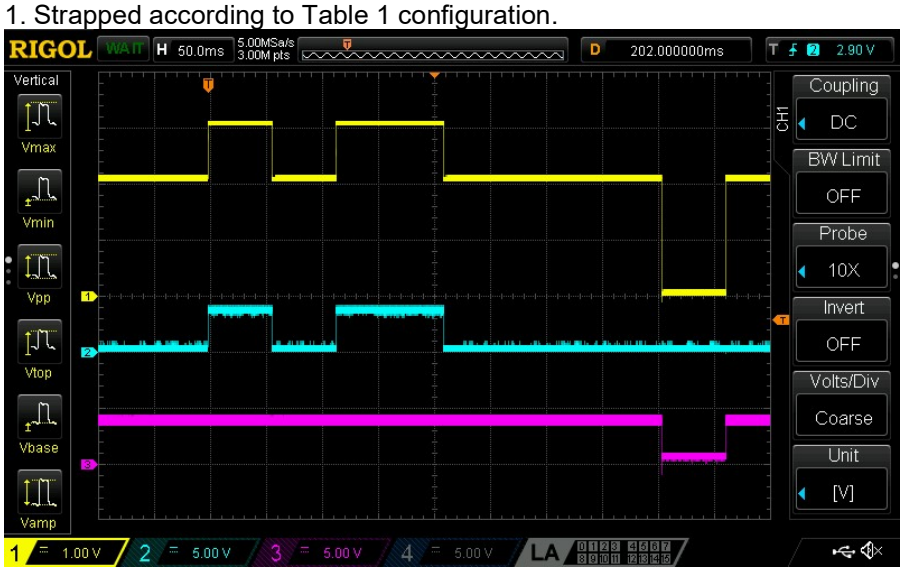
Typical Application Circuit



Functionality Waveforms

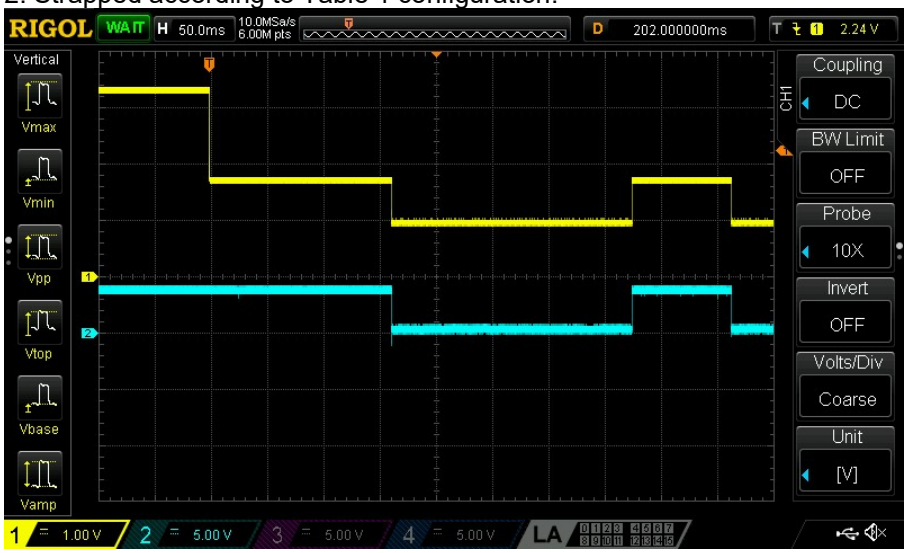
Channel 1 (yellow/top line) – PIN#10 (INT_RSTn)
Channel 2 (light blue/2nd line) – PIN#12 (M_INT)
Channel 3 (magenta /3rd line) – PIN#14 (M_RSTn) with external 5kΩ pull up resistor

1. Strapped according to Table 1 configuration.

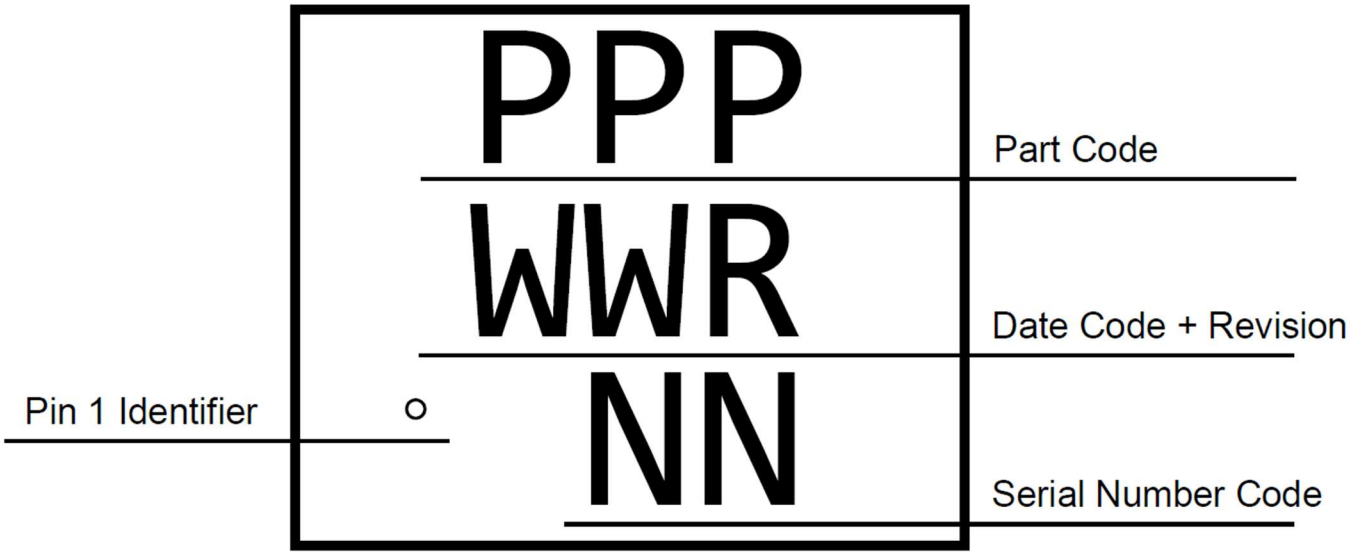


Channel 1 (yellow/top line) – PIN#9 (LPWn_PRSn)
Channel 2 (light blue/2nd line) – PIN#07 (M_LPWn) with external 5kΩ pullup

2. Strapped according to Table 1 configuration.



Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.09	005	U	0x69AB0CAA	9NB	D	09/19/2024

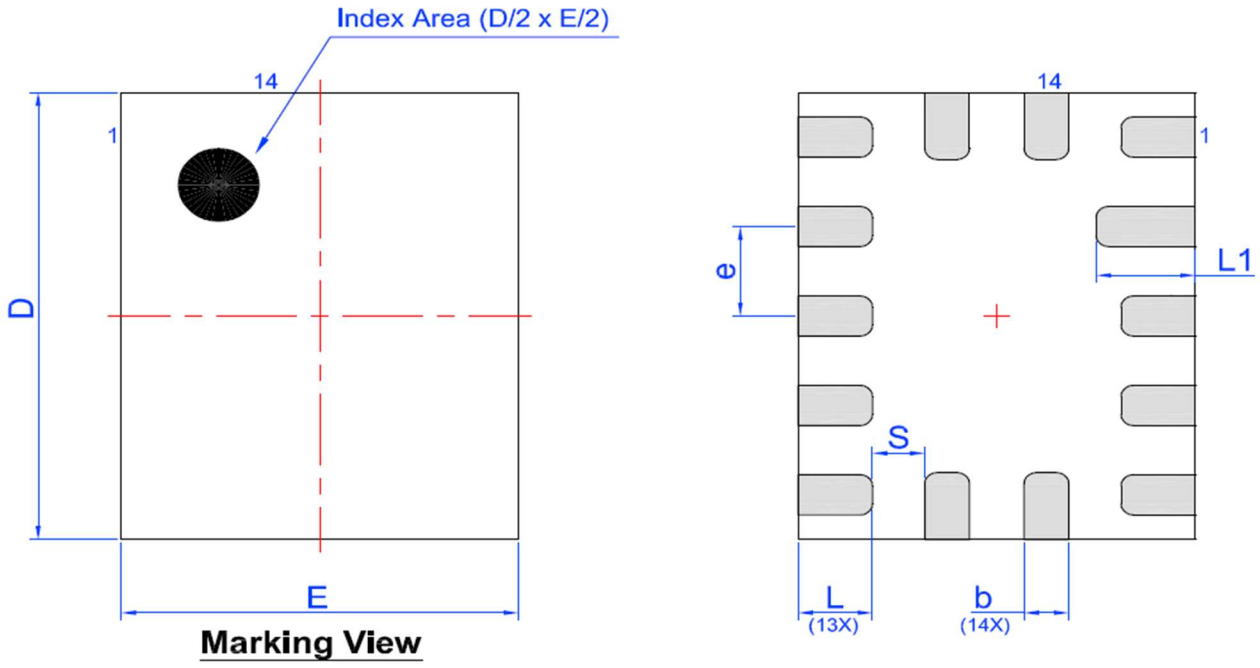
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

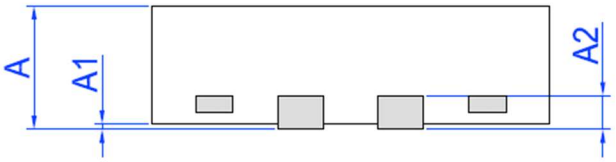
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Marking View



Marking View

Unit: mm

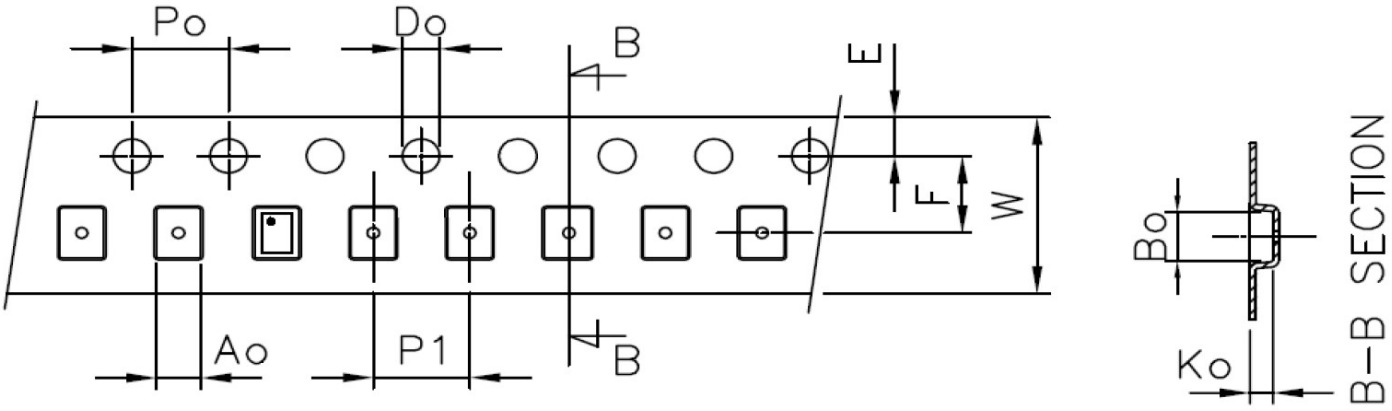
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

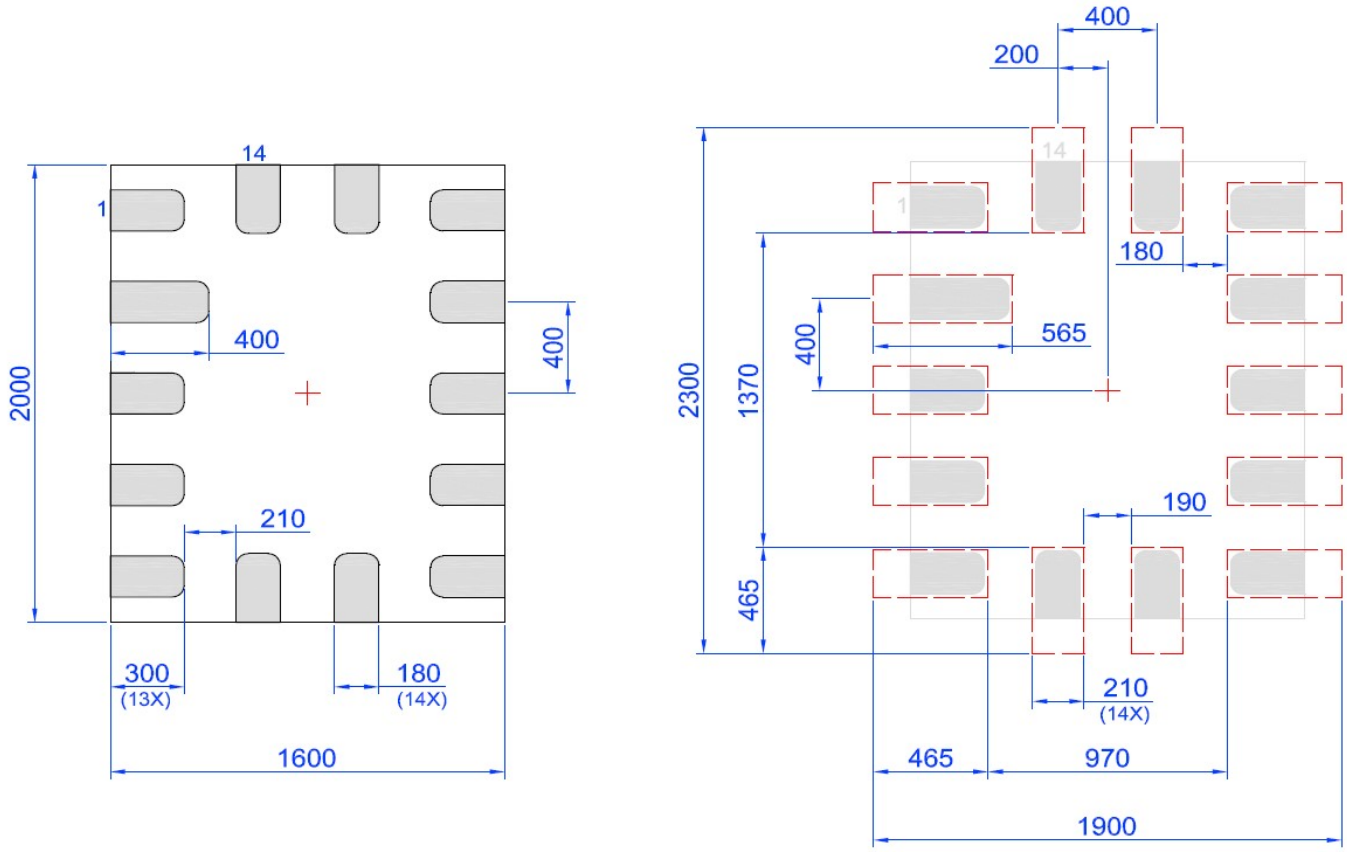
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Layout Guidelines



Unit: um

Datasheet Revision History

Date	Version	Change
03/30/2018	0.10	New design for SLG46855 chip based on SLG4T42331
04/03/2018	0.11	Updated typical application circuit
04/26/2018	0.12	Updated Device Revision Table
06/14/2018	0.13	Updated with GP_r003
06/14/2018	0.14	Updated Device Revision Table
07/03/2018	0.15	Updated device functionality
07/25/2018	0.16	Updated DS formatting and updated temperature sensor
07/25/2018	0.17	Updated Programming Code Number
08/09/2018	0.18	Updated General Description with correct PN
08/17/2018	0.19	Updated Device Revision Table
08/28/2018	0.20	Updated internal resistors information
12/13/2018	0.21	Updated typical application circuit and ACMP threshold voltage range
12/31/2018	0.22	Corrected typos in threshold voltage range, changed current consumption
01/09/2019	1.00	Production Release
01/25/2019	1.01	Updated pin names and application circuit
01/29/2019	1.02	Updated typical application circuit
02/01/2019	1.03	Updated typical application circuit and functionality waveforms
02/05/2019	1.04	Updated Description
02/06/2019	1.05	Updated Description
02/13/2019	1.06	Updated Features to describe the correct OSFP module specification
08/01/2019	1.07	Updated Device Revision Table
12/20/2022	1.08	Moved to Renesas template
09/19/2024	1.09	Updated Top Marking Format and Part Code